



slower rise time and then reshape the output pulse to sharpen it. The cost and volume of the added circuitry can be much less than that of the high figure of merit delay line.

### **SPECIAL TOLERANCES**

Other factors that enter into the cost are special tolerances on delay, impedance, temperature coefficient of delay, distortion and attenuation. The tolerance on tap delays, if too tight, can require the use of more sections than would be required for the desired figure of merit. It is usually preferred that minimum and/or maximum figures be used to specify tolerance limits.

### **DISTORTION**

Standard delay lines have typically less than 15% distortion. Special low-distortion delay lines can be designed at a higher cost. For critical distortion requirements, input rise time should be specified.

### **INSERTION LOSS OR ATTENUATION**

Attenuation on most standard delay lines will run 1% to 3%. Where very low insertion loss is required, it is generally more economical to suffer a higher loss in the delay line and make up for it in the related circuitry, than to make the line highly efficient.

### **CHARACTERISTIC IMPEDANCE**

The line impedance is determined by the source and load impedances of the associated circuits. The trend has been toward lower impedances in the order of 50 to 250 ohms for proper matching to I.C.'s. A good rule of thumb is lower impedances (50 - 500 ohms) for lumped lines, and higher impedances (200 - 1000 ohms) for distributed lines. There are always exceptions, of course. The higher impedance lines with faster rise times have small values of capacitance per section, thus they are difficult to match at the output and are more sensitive to tap loading. Even a few picofarads load capacitance will present a serious mismatch to the high frequency components of the input signal.

## **DESIGN CONSIDERATIONS FOR ACTIVE DELAY NETWORKS**

An active delay network is a combination of a passive delay line and an integrated circuit logic device in a single package. The I.C. device may perform only a simple buffering function, or could provide any of a wide variety of logic functions in conjunction with a delay line, such as a one-shot multi-vibrator, oscillator, or programmable delay network.

### **ADVANTAGES OF ACTIVE DELAY NETWORKS OVER PASSIVE DELAY LINES**

1. Greater function in less board space, due to a reduced number of components.
2. Built-in compensation for I.C. propagation delays.
3. Not significantly affected by external loading.
4. Fixed rise time, independent of delay time.
5. Direct interface with other logic devices — TTL, ECL, or CMOS.

### **SPECIFYING ACTIVE DELAY NETWORKS**

The environment in which an active delay line operates can have an effect on the performance of the unit. In order for POLARA to supply a device that will operate properly in use, the following conditions should be specified:

- Input pulse width, rise time, and repetition rate
- Vcc operating range
- Operating and storage temperature ranges
- Output load conditions
- Positive or negative edge operation

In addition, the following device characteristics should be specified:

- Delay times and tolerances
- Maximum delay variation with temperature

If a standard delay network is not appropriate for a certain requirement, POLARA can produce a special unit to provide the characteristics needed. Our engineering department is available to provide design assistance for special requirements and applications.