POLARA

IMPEDANCE

All passive delay lines must be terminated into their characteristic impedance. The characteristic impedance of a delay line is the value of the terminating resistance that results in the minimum reflection back toward the delay line input. Impedance Z_O is measured in ohms and is expressed as $Z_O = \sqrt{L/C}$.

RISE TIME

The rise time of a delay determines the faithfulness of reproduction of the input pulse. The high frequency response of a delay line is related to the resonant frequency and Q of the individual sections. An increase in the number of sections for a given delay and impedance reduces the section L and C values, thus increasing F_C. The line rise time (T_R) and the delay line cutoff frequency (F_C) are related as follows:

$$F_C(3dB) = \frac{360}{T_R} \qquad F_C = MHz, \qquad T_R = nsec$$

The line rise time is related to the input and output pulse rise times by the equation:

$$T_R = \sqrt{T_{RO}^2 - T_{RI}^2}$$

where T_R = line rise time
T_{RO} = output pulse rise time
T_{RI} = input pulse rise time

The number of sections required for a lumped constant delay line to achieve a specified delay T_D with a rise time T_R is proportional to $(T_D / T_R)^{(1/4)}$ From this expression, it is apparent that the choice of rise time has a significant effect on the required number of sections and, therefore, on size and cost.

ATTENUATION

Attenuation in a delay line is the amplitude difference between input and output signals. Attenuation or insertion losses in a delay line are caused primarily by the dc resistance of the inductor windings. Dielectric, ground plane and other losses can, for practical purposes, be ignored on a lumped constant delay line.

EXTERNAL CIRCUIT ENVIRONMENT CONSIDERATIONS

For delays $\leq$ 20 nsec and line rise times $\leq$ 4 nsec, special care must be taken to provide extensive ground planes on the PC Board and allow for extra ground pins on the delay line.
In addition, these delay lines can be easily overloaded by load capacitance at the taps. All delay line resistive tap loads should be $\geq 10 \times Z_O$. The capacitance portion of any load should be $\leq$ 10% of the delay line section capacitor value. The equation for section capacitor value for any delay line is:

$$C_S = \frac{1000\, T_D}{n\, Z_O}$$

where n = number of sections
T_D = total delay (nsec)
Z_O = characteristic impedance (ohms)

For situations where the capacitive tap loading exceeds 10% of the section capacitance, special designs can be created to reduce the internal capacitor by that amount.

COST CONSIDERATIONS FOR PASSIVE DELAY LINES

NUMBER OF SECTIONS

The size of a delay line is directly proportional to the number of sections or components required to satisfy the T_D/T_R, or figure of merit. Consequently, the cost of the delay line will be significantly effected by the choice of the ratio of total delay to line rise time. It is usually more economical to accept a delay line of

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